



higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

6 August 2026

This marking guideline consists of 6 pages.

QUESTION 1

- 1.1 1.1.1 Binary
 1.1.2 Binary adder
 1.1.3 16
 1.1.4 AND
 1.1.5 Binary conversion

(5 × 1) (5)

- 1.2 1.2.1

$$\begin{array}{r}
 10111 \\
 + 10011 \\
 + 10101 \\
 \hline
 = 11111 \quad \checkmark
 \end{array}$$

$$11111_2 = 63_{10} \quad \checkmark \checkmark$$

(3)

- 1.2.2

$$\begin{array}{r}
 1101 \\
 101 \\
 \hline
 1101 \\
 + 0000 \quad \checkmark \\
 + 1100 \\
 \hline
 = 100001 \quad \checkmark \checkmark
 \end{array}$$

1	000	001
1	0	1

$$1000001_2 = (101)_8 \quad \checkmark \checkmark$$

(5)

- 1.2.3

$$\begin{array}{r}
 110 \quad 10101 \quad \checkmark \\
 \hline
 110 \quad 111110 \\
 110 \\
 \hline
 111 \\
 110 \\
 \hline
 110 \\
 110 \quad \checkmark \checkmark \\
 \hline
 2^4 \quad 2^3 \quad 2^2 \quad 2^1 \quad 2^0 \\
 1 \quad 0 \quad 1 \quad 0 \quad 1
 \end{array}$$

$$32 + 0 + 8 + 0 + 2 = (42)_{10} \quad \checkmark \checkmark$$

(5)

- 1.3 1.3.1 Full Adder

(1)

- 1.3.2 Co = Carry out ✓
 S = Sum ✓

(2)

- 1.3.3 OR gate

(1)

1.3.4

A	B	Cin	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
		✓	✓	✓

(3)
[25]

QUESTION 2

- 2.1 2.1.1 A
 2.1.2 B
 2.1.3 B
 2.1.4 A
 2.1.5 B

(5 × 1) (5)

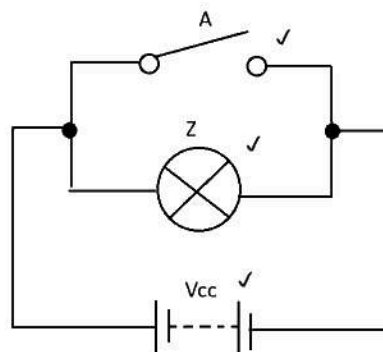
- 2.2
- An encoder converts multiple input lines into a coded binary output and a decoder converts a coded binary input into multiple output lines.
 - Encoders reduce many inputs into fewer outputs and decoders expand fewer inputs into many outputs.
 - Encoders are used for data compression, while decoders are used for data expansion/display.

(Any 2 × 1) (2)

- 2.3
- Keyboards (encoding key presses into binary)
 - Digital calculators
 - Seven-segment displays (decoder usage)
 - Memory address decoding in computers
 - Digital communication systems
 - Traffic light control systems
 - Barcode scanners

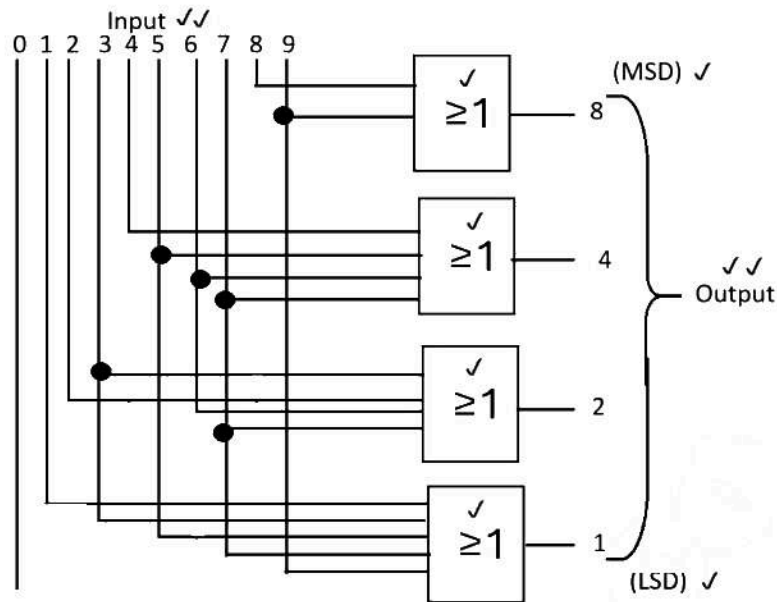
(Any 5 × 1) (5)

2.4



(1 mark for each component if the circuit is drawn correctly.)

2.5



(10)
[25]

QUESTION 3

- 3.1 3.1.1 True
 3.1.2 False
 3.1.3 False
 3.1.4 True
 3.1.5 False

(5 × 1) (5)

- 3.2 3.2.1 Clocked SR flip-flop

(2)

3.2.2

Clock	S	R	Q(next)	Operation
1	0	0	Q	No change ✓
1	0	1	0	Reset ✓
1	1	0	1	Set ✓
1	1	1	Invalid	Forbidden condition ✓

(4)

- 3.2.3 SD (Set Direct): Sets the output Q to 1 directly.
 RD (Reset Direct): Resets the output Q to 0 directly.

(2)

- 3.3 • Access time
 • Storage capacity
 • Speed
 • Volatility
 • Power consumption
 • Cost per bit
 • Reliability

(Any 5 × 1) (5)

3.4 a) J = 1 and K = 0 (2)

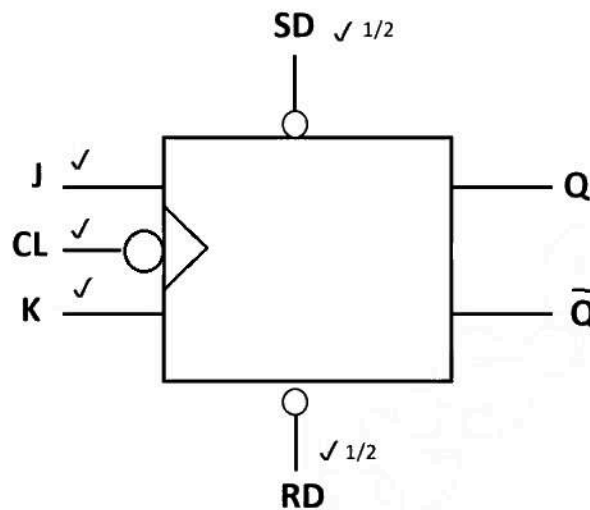
The flip-flop is SET, ✓ and the output Q becomes 1. ✓

b) J = 0 and K = 1 (2)

The flip-flop is RESET, ✓ and the output Q becomes 0. ✓

(2)

3.5



(5)
[25]

QUESTION 4

- 4.1.1 B
- 4.1.2 A
- 4.1.3 D
- 4.1.4 C
- 4.1.5 E

(5 × 1) (5)

- 4.2 4.2.1
- A shift register is a digital circuit used to store and shift binary data from one flip-flop to another.
 - A shift register is a group of flip-flops connected in series that is used to store and move binary data either left or right one bit at a time with each clock pulse.

4.2.2 The clock pulse controls the shifting of binary data from one stage to the next in the shift register.

4.2.3 After each clock pulse, the binary data shifts one position to the right from one flip-flop to the next.

(3 × 2) (6)

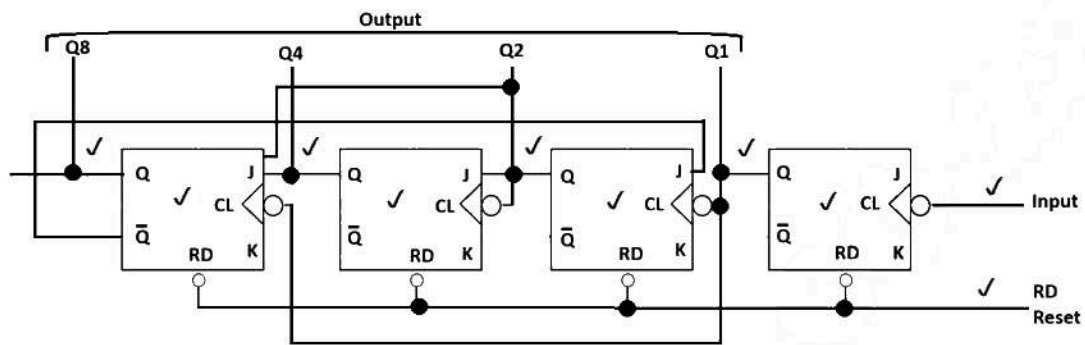
4.3

ASYNCHRONOUS COUNTER	SYNCHRONOUS COUNTER
Flip-flops do not receive the clock pulse simultaneously.	All flip-flops receive the clock pulse simultaneously.
Slower in operation due to propagation delay.	Faster in operation.

(2 × 2)

(4)

4.4



(10)

[25]

TOTAL:

100