



higher education & training

Department:
Higher Education and Training
REPUBLIC OF SOUTH AFRICA

MARKING GUIDELINE

NATIONAL CERTIFICATE

LOGIC SYSTEMS N2

4 April 2024

This marking guideline consists of 5 pages.

QUESTION 1

- 1.1. 1.1.1 Decimal number system
 1.1.2 Binary number system
 1.1.3 Octal number system
 1.1.4 Hexadecimal number system

(4 × 1) (4)

- 1.2. Binary number system

(1)

- 1.3. 1.3.1 $11011_2 + 1110_2 + 1010_2$

$$\begin{array}{r}
 1 \quad 1 \quad 0 \quad 1 \quad 1 \quad \checkmark \\
 \quad \quad 1 \quad 1 \quad 1 \quad 0 \\
 + \quad \quad 1 \quad 0 \quad 1 \quad 0 \\
 \hline
 1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 1 \quad \checkmark
 \end{array}$$

$$\begin{aligned}
 110011_2 &= 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 \checkmark \\
 &= 32 + 16 + 0 + 0 + 2 + 1 \\
 &= 51_{10} \checkmark
 \end{aligned}$$

(4)

- 1.3.2 $11001_2 - 1011_2$

$$\begin{array}{r}
 \quad \quad 1 \quad 1 \quad 0 \quad 0 \quad 1 \quad \checkmark \\
 - \quad \quad 1 \quad 0 \quad 1 \quad 1 \\
 \hline
 \quad \quad 1 \quad 1 \quad 1 \quad 0 \quad \checkmark
 \end{array}$$

$$\begin{aligned}
 1110_2 &= 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 \checkmark \\
 &= 8 + 4 + 2 + 0 \\
 &= 14_{10} \checkmark
 \end{aligned}$$

(4)

- 1.3.3 $1111010_2 \div 110010_2$

$$\begin{array}{r}
 \quad \quad \quad \quad \quad 1 \quad 0 \quad 1 \quad \checkmark \\
 1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 0 \quad \boxed{1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 0 \quad 1 \quad 0} \quad \checkmark \\
 - \quad \quad \quad 1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 0 \\
 \hline
 \quad \quad \quad \quad 1 \quad 1 \quad 0 \quad 0 \quad 1 \\
 - \quad \quad \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad \checkmark \\
 \hline
 \quad \quad \quad \quad 1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 0 \\
 - \quad \quad \quad 1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 0 \quad \checkmark \\
 \hline
 \quad \quad \quad \quad \quad \quad 0 \quad 0
 \end{array}$$

$$\begin{aligned}
 101_2 &= 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 \checkmark \\
 &= 4 + 0 + 1 \\
 &= 5_{10} \checkmark
 \end{aligned}$$

(6)

1.4.1 FULL ADDER ✓✓

(2)

1.4.2

- The first half adder obtains the sum of inputs A and B. ✓
- The second half adder obtains the sum of the inputs Cin and first half adder's sum. ✓
- Then the carry out of the first adder is to the carry out of the second half adder through an OR gate to obtain the full adder's carry out. ✓
- Finally the sum output of the second half adder is the sum of the full adder. ✓

(4)

1.4.3

A	B	B _{in}	D	B _o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

✓ ✓

(2)

[25]

QUESTION 2

2.1

Weighted code is a code by which the value of the position of every binary digit can be specified.

(2)

2.2

8421 code
4221 code
2421 code
5211 code
5421 code

(Any 3 × 1)

(3)

2.3

Decimal digits	2421 BCD code
0	0000
1	0001
2	0010
3	0011
4	0100
5	1011
6	1100
7	1101
8	1110
9	1111

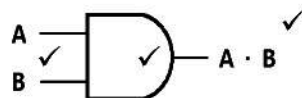
✓
✓
✓
✓
✓
✓
✓
✓
✓
✓

- 2.4 Step 1 – A decimal number is punched on the key pad. ✓
 Step 2 – The ENCODER changes the decimal number into a binary number
 ✓ which is acceptable to the PROCESSOR. ✓
 Step 3 – the DECODER then changed the Binary number into a form that can
 be displayed on the screen. ✓ (4)
- 2.5
- Data conversion
 - Data transmission
 - Data expansion
 - Data error detection and correction (4)
- 2.6
- ASCII code
 - EBCDIC code
 - GRAY CODE
 - Hamming code
 - BCD code
 - Excessive 3code
- (Any 2 × 1) (2)
[25]

QUESTION 3

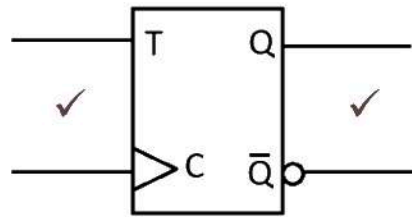
- 3.1 A memory device is any device that can store logic 1 and logic 0 bits ✓ in such
 a way that a single bit or group of bits ✓ is available and can be re-obtained. ✓ (3)
- 3.2
- Main memory or volatile memory
 - Secondary memory or non-volatile memory (2 × 1) (2)
- 3.3 The output of a NOR gate will be a logic 1 only if all the inputs are at logic 0, ✓
 otherwise the output will be a logic 0. ✓ (2)
- 3.4
- OR gate ✓ and
 - NOT gate ✓ (2)
- 3.5 3.5.1
- C is XOR gate
 - D is AND gate
 - E is NOR gate (3)

3.5.2



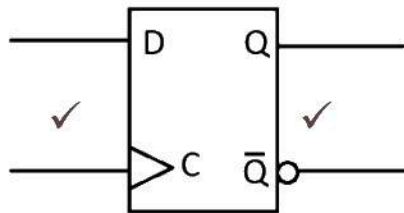
(3)

3.6 3.6.1



(2)

3.6.2



(2)

3.7

- T = 0 (Low): The T flip-flop holds its current state. ✓
- T = 1 (High): The T flip-flop toggles its output state. ✓
- The clock signal controls when the T flip-flop changes its state based on the T input. ✓
- The state change occurs on the rising edge or falling edge of the clock pulse, depending on the specific design of the flip-flop. ✓
- Q: Represents the output of the flip-flop. ✓
- Q': Represents the complement of the Q output. This means Q' is always the opposite of Q. ✓

(6)
[25]

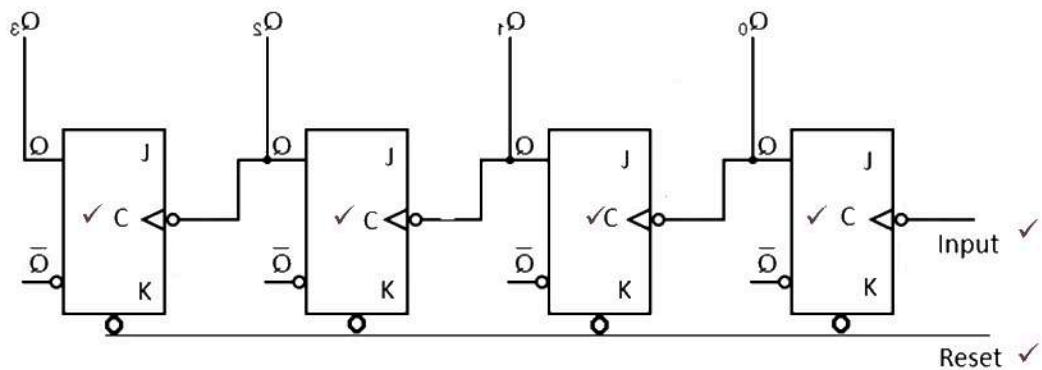
QUESTION 4

4.1

- A counter is an electronic circuit which executes the counting function ✓ by counting the number of pulses applied to the input. ✓
- A shift register is a memory in which information (data) is moved or shifted one position at a time, ✓ in response to an applied clock pulse. ✓

(4)

4.2.1



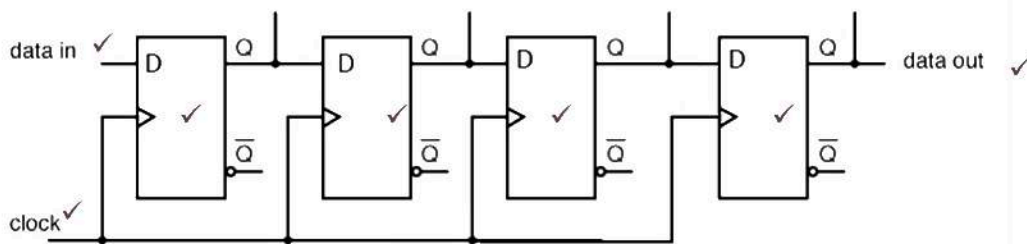
(6)

4.2.2

- Initially, all flip-flops will be in the reset state ($Q = 0$). ✓
- With the first clock pulse, Q_0 changes to 1, while Q_1 and Q_2 remain 0. ✓
- With the second clock pulse, Q_0 remains 1, Q_1 changes to 1 due to the change in Q_0 , and Q_2 remains 0. ✓
- This sequence continues, with each clock pulse changing the state of the flip-flop ✓

(4)

4.3



(7)

4.4 4.4.1 False ✓

(1)

4.4.2 True ✓

(1)

4.4.3 True ✓

(1)

4.4.3 False ✓

(1)

[25]

TOTAL: 100